REMARKS

Entry of this Amendment is proper since it narrows the issues on appeal and does not require further search by the Examiner.

Claims 11-18 and 26-31 and 33-35 and 37-43 are all the claims presently pending in the application. Claim 36 has been canceled. Claims 11, 26, 37 and 38 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 11-12, 18, 26, 28, 33, 36, 38-41 and 43 stand rejected under 35 U.S.C. § 102(e) being allegedly anticipated by Lee et al. (U.S. Patent No. 5,895,947). Claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 36-38 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam, et al. (U.S. Patent No. 5,940,319) and Lee. Claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam and Lee and further in view of Bronner et al. (U. S. Patent No. 6,242,770).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (as recited in claim 11) is directed to an array of microelectronic elements which includes a substrate of semiconductor material, a lower layer of dielectric material disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto, a pattern of mutually electrically isolated conductive regions disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer, and a plurality of nodes of semiconductor material disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer. Each conducting region may

include a metal conductor, and a via which is filled with a diffusion barrier material, the diffusion barrier material extending between the metal conductor and a node in said plurality of nodes and electrically connecting the metal conductor with the node.

Importantly, the array also includes a bonding promoting layer formed on the lower layer of dielectric material, the bonding promoting layer bonding the lower surface of the upper layer of dielectric material to the upper surface of the lower layer.

Conventional devices typically form a semiconductor node (e.g., a silicon diode) directly on an aluminum or copper metal conductor (e.g., a word line) (e.g., as illustrated in Figure 17 of the Durlam reference). However, such devices suffer severe problems. Namely, the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.

To address this problem, the metal conductor (e.g., word line) may be made from a refractory metal. However, such refractory metal word lines have a high resistance, such that only small arrays of memory elements can be made (Application at page 8, lines 10-13).

The claimed invention, on the other hand, forms, in a lower dielectric layer, a via on a metal conductor which is filled with a diffusion barrier material, and forms, in an upper dielectric layer, a plurality of nodes (e.g., Application at Figure 5B). Further, a bonding promoting layer is formed on the lower dielectric layer, the bonding promoting layer bonding the upper dielectric layer to the lower dielectric layer (Application at 13, lines 9-12). The bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

II. THE PRIOR ART REFERENCES

A. The Lee Reference

The Examiner alleges that Lee teaches the claimed invention as recited in claims 11-12, 18, 26, 28, 33, 36, 38-41 and 43. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Lee.

Contrary to the Examiner's allegations, Lee does not teach or suggest "*a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper*

surface of said lower layer", as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, unlike conventional devices, the claimed invention forms, in a lower dielectric layer, a via on a metal conductor which is filled with a diffusion barrier material, and forms, in an upper dielectric layer, a plurality of nodes (e.g., Application at page 8, lines 3-16; Figure 5B). Further, a bonding promoting layer is formed on the lower dielectric layer, the bonding promoting layer bonding the upper dielectric layer to the lower dielectric layer (Application at page 13, lines 9-12).

In particular, the bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

Clearly, Lee does not teach or suggest these novel features. Indeed, Lee does not even disclose any bonding process but merely teaches depositing layer on top of layer, and so on (e.g., see Figures 2-8 of Lee). Certainly, Lee does not teach or suggest a bonding promoting layer which bonds first and second dielectric layers.

Indeed, the Examiner surprisingly attempts to equate the second capping layer 134 with the bonding promoting layer of the claimed invention. However, this is completely unreasonable.

In fact, Lee teaches that the second capping layer is made of Si_3N_4 (Lee at col. 5, lines 8-10). Further, the capping layer 134 is formed between the oxide film 130 and the dielectric film 140. Importantly, nowhere does Lee teach or suggest that the layer 134 may include some form of "bonding promotion characteristic". In fact, Lee provides no support for the Examiner's surprising statement that the layer 134 is a bonding promoting layer. Indeed, **the Examiner appears to have simply fabricated this characteristic out of thin air, on a whim, in a desperate attempt to support his allegations.**

Moreover, Applicant would point out that nowhere does Lee teach or suggest that layer 140 is bonded to layer 130. In fact, Lee only teaches that the layer 140 is "formed by forming an insulating film such as an oxide film on the entire surface of the resultant structure ... and removing the insulating film by etching the insulating film in the cell array region using the second capping layer 134 as an etch stop layer" (Lee at col. 5, lines 49-56). That is, Lee certainly does not teach that layer 140 is bonded to layer 130. Therefore, clearly there

is no need for a "bonding promoting layer" as unreasonably suggested by the Examiner.

Further, Applicant would point out that by definition, a bonding promoting layer is a layer that promotes bonding. The term "promote" may be defined as "to contribute to the growth or prosperity of" (*Webster's Universal Encyclopedic Dictionary*, Barnes and Noble Books (2002), p. 1464). Applicant respectfully submits that the layer 134 does not promote the bonding of layers 130 and 140. Indeed, there is no reason to suggest that the bond between layers 130 and 140 is any stronger because of layer 134, than if layer 134 was omitted entirely.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Lee. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Durlam Reference

The Examiner alleges that Durlam would have been combined with Lee to form the invention of claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 36-43. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant respectfully submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant submits that the Examiner fails to identify any motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, these references clearly do not teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Durlam, nor Lee, nor any alleged combination thereof, teaches or suggests "*a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer*", as recited, for example, in claim 11 and

similarly recited in claims 26 and 38.

As noted above, unlike conventional devices, in the claimed invention, a bonding promoting layer is formed on the lower dielectric layer, the bonding promoting layer bonding the upper dielectric layer to the lower dielectric layer (Application at page 13, lines 9-12). The bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

Clearly, Durlam does not teach or suggest these novel features. Indeed, the Examiner surprisingly attempts to equate the dielectric layer 33 with the bonding promoting layer of the claimed invention. However, this is clearly unreasonable.

Indeed, the Examiner recognizes in the Office Action that the dielectric layer 33 "is placed between the lower layer 25 and the upper layer 51 to provide electrical isolation between the conductor layers". The Examiner **amazingly** goes on to state that since the bonding promoting layer in the claimed invention can include glass, and since glass may provide electrical isolation, that it "would have been obvious to form the dielectric layer 33 as a glass layer because the glass layer would also provide the electrical isolation between the conductor layers" (Office Action at page 6). Applicant respectfully submits that **the Examiner's argument here is complete nonsense and does not even justify a response**.

However, Applicant will point out that the Examiner does not even attempt to allege that the layer 33 is intended to have any type of "bonding promoting" characteristic. Indeed, the layer 33, as the Examiner correctly points out, is merely intended to provide electrical isolation. In fact, nowhere does Durlam teach or suggest that conductor layer 34 is "bonded to" the digit lines 29 and 30, but merely states that the layer 34 is "deposited". Thus, there is no need for a "bonding promoting layer" in Durlam.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Bronner Reference

The Examiner alleges that the alleged Durlam/Lee combination would have been

further combined with Bronner to form the claimed invention as recited in claims 13-14, 17, 27 and 30-31. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant respectfully submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant submits that the Examiner fails to identify any motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, these references clearly do not teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Durlam, nor Lee, nor Bronner, nor any alleged combination thereof, teaches or suggests "*a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer*", as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, the bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

Clearly, Bronner does not teach or suggest these novel features. Indeed, the Examiner is merely relying on Bronner as allegedly teaching another feature of the claimed invention and does not allege that Bronner teaches or suggests this feature.

Further, Bronner merely merely discloses a diode 514 which is in the shape of a V-groove formed in an insulation layer 100. A metal conductor 525 is formed on the diode 514 and an oxide layer 530 is formed on the metal conductor 525 (Bronner at Figure 5B). This structure is completely unrelated to the claimed invention.

In fact, like Lee and Durlam, nowhere does Bronner teach or suggested a second dielectric layer bonded to a first dielectric layer. Therefore, Bronner certainly does not teach

or suggest a bonding promoting layer. Thus, Bronner clearly does not make up for the deficiencies of Durlam and Lee.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 11-18 and 26-31 and 33-35 and 37-43, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 2/28/05

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